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EXAMINER	
HO, CHUONG T	

ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 12/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/764,656	SILVERMAN ET AL.	
	Examiner	Art Unit	
	Chuong Ho	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-22 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-8,10-14,16-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rochberger et al. (U.S.Patent No. 6,760,309 B1) in view of Dravida et al. (U.S. Patent No. 2002/0105965 A1).

In the claim 10, see figure 6, Rochberger et al. discloses the device 100 may comprise a plurality of time delay sensitive queues whereby each class (precedence levels) has associated with it one or more queues. In the example illustrated in FIG.6, class #1 through class #4 each have a single queue associated with them (see col. 12, lines 34-36); comprising:

Determining the buffer size for transmitting information over the communication network (see col. 12, lines 34-36, the device 100 may comprise a plurality of time delay sensitive queues whereby each class (precedence levels) has associated with it one or more queues. In the example illustrated in FIG.6, class #1 through class #4 each have a single queue associated with them) (see col. 12, lines 42-55, the order of retrieving packets from the queues 106, 108 is related to the various priority levels previously assigned to the packets. The processing resources of the processor 114 are distributed

in some form among all the queues vying for service. To distribute processing resource, each queue is assigned a percentage of the processing capacity of the processor 114. For example, assuming 100% available resources, the time delay sensitive queues may be assigned a combined 80% of the resource while the non-delay sensitive queues are assigned the remaining 20%. The 80% can then be further broken down by priority level: class #4 corresponding to priority level P4, is assigned 5% of processing resources; class #3, corresponding to priority level P3, is assigned 10%; class #2, corresponding to priority level P2, is assigned 15%; and class #1, corresponding to priority level P1, is assigned 50%....the non-delay sensitive queue is assigned 20% of the processing resources);

Determining a plurality of precedence levels (class #1 through class #4) for at least a portion of information (packets) passing over communication network (see col. 12, lines 42-55, the order of retrieving packets from the queues 106, 108 is related to the various priority levels previously assigned to the packets. The processing resources of the processor 114 are distributed in some form among all the queues vying for service. To distribute processing resource, each queue is assigned a percentage of the processing capacity of the processor 114. For example, assuming 100% available resources, the time delay sensitive queues may be assigned a combined 80% of the resource while the non-delay sensitive queues are assigned the remaining 20%. The 80% can then be further broken down by priority level: class #4 corresponding to priority level P4, is assigned 5% of processing resources; class #3, corresponding to priority level P3, is assigned 10%; class #2, corresponding to priority level P2, is assigned 15%; and class

#1, corresponding to priority level P1, is assigned 50%....the non-delay sensitive queue is assigned 20% of the processing resources);

Assigning a percentage of buffer to each of precedence levels (class #1 through class #4), wherein the sum of percentage may exceed 100% (see col. 12, lines 42-55, the order of retrieving packets from the queues 106, 108 is related to the various priority levels previously assigned to the packets. The processing resources of the processor 114 are distributed in some form among all the queues vying for service. To distribute processing resource, each queue is assigned a percentage of the processing capacity of the processor 114. For example, assuming 100% available resources, the time delay sensitive queues may be assigned a combined 80% of the resource while the non-delay sensitive queues are assigned the remaining 20%. The 80% can then be further broken down by priority level: class #4 corresponding to priority level P4, is assigned 5% of processing resources; class #3, corresponding to priority level P3, is assigned 10%; class #2, corresponding to priority level P2, is assigned 15%; and class #1, corresponding to priority level P1, is assigned 50%....the non-delay sensitive queue is assigned 20% of the processing resources);

Receiving an information packets, packet having a label (class 178, 198, see figures 9, 10) indicating the precedence (class#1 through class#4) for transmitting information (see figure 6) (see col. 12, lines 34-36, the device 100 may comprise a plurality of time delay sensitive queues whereby each class (precedence levels) has associated with it one or more queues. In the example illustrated in FIG.6, class #1 through class #4 each have a single queue associated with them) (see col. 12, lines 42-55, the order of

retrieving packets from the queues 106, 108 is related to the various priority levels previously assigned to the packets. The processing resources of the processor 114 are distributed in some form among all the queues vying for service. To distribute processing resource, each queue is assigned a percentage of the processing capacity of the processor 114. For example, assuming 100% available resources, the time delay sensitive queues may be assigned a combined 80% of the resource while the non-delay sensitive queues are assigned the remaining 20%. The 80% can then be further broken down by priority level: class #4 corresponding to priority level P4, is assigned 5% of processing resources; class #3, corresponding to priority level P3, is assigned 10%; class #2, corresponding to priority level P2, is assigned 15%; and class #1, corresponding to priority level P1, is assigned 50%....the non-delay sensitive queue is assigned 20% of the processing resources);

Examining the label (class 178, 198, see figures 9, 10) on packet to determine the precedence level (class #1 through class #4) of packet; evaluating label (class 178, 198, see figures 9, 10) against plurality of precedence levels (class #1 through class #4); and

If the precedence (class 178, 198) of packet matches one of plurality of precedence levels (class #1 through class #4), passing packet for processing in a priority buffer queue (see col. 12, lines 34-36, the device 100 may comprise a plurality of time delay sensitive queues whereby each class (precedence levels) has associated with it one or more queues. In the example illustrated in FIG.6, class #1 through class #4 each have a single queue associated with them) (see col. 12, lines 42-55, the order of retrieving packets from the queues 106, 108 is related to the various priority levels previously

assigned to the packets. The processing resources of the processor 114 are distributed in some form among all the queues vying for service. To distribute processing resource, each queue is assigned a percentage of the processing capacity of the processor 114. For example, assuming 100% available resources, the time delay sensitive queues may be assigned a combined 80% of the resource while the non-delay sensitive queues are assigned the remaining 20%. The 80% can then be further broken down by priority level: class #4 corresponding to priority level P4, is assigned 5% of processing resources; class #3, corresponding to priority level P3, is assigned 10%; class #2, corresponding to priority level P2, is assigned 15%; and class #1, corresponding to priority level P1, is assigned 50%....the non-delay sensitive queue is assigned 20% of the processing resources);

If the precedence of packet does not match one of plurality of precedence level (class #1 through class #4), passing packet for processing in at least one other output queue (non-delay sensitive queue, see figure 6) (see col. 12, lines 34-36, the device 100 may comprise a plurality of time delay sensitive queues whereby each class (precedence levels) has associated with it one or more queues. In the example illustrated in FIG.6, class #1 through class #4 each have a single queue associated with them) (see col. 12, lines 42-55, the order of retrieving packets from the queues 106, 108 is related to the various priority levels previously assigned to the packets. The processing resources of the processor 114 are distributed in some form among all the queues vying for service. To distribute processing resource, each queue is assigned a percentage of the processing capacity of the processor 114. For example, assuming 100% available

resources, the time delay sensitive queues may be assigned a combined 80% of the resource while the non-delay sensitive queues are assigned the remaining 20%. The 80% can then be further broken down by priority level: class #4 corresponding to priority level P4, is assigned 5% of processing resources; class #3, corresponding to priority level P3, is assigned 10%; class #2, corresponding to priority level P2, is assigned 15%; and class #1, corresponding to priority level P1, is assigned 50%....the non-delay sensitive queue is assigned 20% of the processing resources);

However, Rochberger et al. is silent to disclosing determining a maximum packet size; if the received information packet exceeds the maximum packet size, discarding the packet.

See figure 28, Dravida et al. (U.S.Patent No. 2002/0105965 A1 "Provisional application No. 60/234,682, filed on Sep. 22, 2000") discloses there are four QoS classes (precedence levels) in the embodiment of the Access Network, there are four egress buffers—one for each class—in each NIU. Each egress buffer is allocated a fixed amount of space to hold packets. The egress buffer control stage 1310 performs a simple operation. When a packet is handed to this stage, it checks if the egress buffer associated with the packet's QoS class (which is a function of its service instance) has adequate space (in term of byte count) to hold the packet, see page 18, [0258]); comprising:

determining a maximum packet size; if the received information packet exceeds the maximum packet size, discarding the packet (see page 18, [0025], packet size restriction can also be enforced at this stage. For instance, if a service instance is set up

with a limit on the maximum packet size, a packet belonging to that service instance can be dropped at this stage if it size exceeds the corresponding limit...packet size restrictions may be enforced at the traffic policing stage).

Thus, it would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Rocchberger with the teaching of Dravida to determine a maximum packet size; if the received information packet exceeds the maximum packet size, discarding the packet in order to speed up forwarding.

3. In the claim 11, Dravida discloses determining if buffer includes packets having precedence level (space level) up to the percentage of buffer assigned to the precedence of packet, if the percentage of buffer assigned to the precedence of information has been filed, discarding packet (in the embodiment of the Access Network, there are four egress buffers—one for each class—in each NIU. Each egress buffer is allocated a fixed amount of space to hold packets. The egress buffer control stage 1310 performs a simple operation. When a packet is handed to this stage, it checks if the egress buffer associated with the packet's QoS class (which is a function of its service instance) has adequate space (in term of byte count) to hold the packet. If it does, the packet is placed in that buffer where it waits for its turn at transmission. Otherwise, it is dropped, see page 18, [0258]).

4. In the claims 12, 2, 3, 18, 19, 21, 22, Dravida discloses the step of processing packet in at least one other output buffer queue ((non-delay sensitive queue) further comprises the step of:

Determining if buffer is full, discarding (dropping) packet; and if the buffer is not full, adding packet to a non-priority queue for transmission packet (in the embodiment of the Access Network, there are four egress buffers—one for each class—in each NIU. Each egress buffer is allocated a fixed amount of space to hold packets. The egress buffer control stage 1310 performs a simple operation. When a packet is handed to this stage, it checks if the egress buffer associated with the packet's QoS class (which is a function of its service instance) has adequate space (in term of byte count) to hold the packet. If it does, the packet is placed in that buffer where it waits for its turn at transmission. Otherwise, it is dropped, see page 18, [0258]).

5. In the claim 13, Dravida discloses transmitting the packets from the priority queue before transmitting the packets for the other output queue (see page 19, [0277], after finishing copying a packet into a transmit buffer, the scheduler scans the input queues going from the highest priority to the lowest priority queue to see which is the highest priority packet waiting at the head of its queue which is ready for transmission).

6. In the claim 14, Rochberger et al. discloses information packet includes a packet header and label is included in a field in packet header (see class 178, 198, figures 9, 10).

7. In the claims 16, 4, Rochberger discloses a larger percentage of buffer (50%) is assigned to information with a higher precedence level (class #1) (see col. 12, lines 42-55, the order of retrieving packets from the queues 106, 108 is related to the various priority levels previously assigned to the packets. The processing resources of the processor 114 are distributed in some form among all the queues vying for service. To

distribute processing resource, each queue is assigned a percentage of the processing capacity of the processor 114. For example, assuming 100% available resources, the time delay sensitive queues may be assigned a combined 80% of the resource while the non-delay sensitive queues are assigned the remaining 20%. The 80% can then be further broken down by priority level: class #4 corresponding to priority level P4, is assigned 5% of processing resources; class #3, corresponding to priority level P3, is assigned 10%; class #2, corresponding to priority level P2, is assigned 15%; and class #1, corresponding to priority level P1, is assigned 50%....the non-delay sensitive queue is assigned 20% of the processing resources);

8. In the claims 1, 17, 20, see figure 6, Rochberger et al. discloses the device 100 may comprise a plurality of time delay sensitive queues whereby each class (precedence levels) has associated with it one or more queues. In the example illustrated in FIG.6, class #1 through class #4 each have a single queue associated with them (see col. 12, lines 34-36); comprising:

Determining the buffer size for transmitting information over the communication network (see col. 12, lines 34-36, the device 100 may comprise a plurality of time delay sensitive queues whereby each class (precedence levels) has associated with it one or more queues. In the example illustrated in FIG.6, class #1 through class #4 each have a single queue associated with them) (see col. 12, lines 42-55, the order of retrieving packets from the queues 106, 108 is related to the various priority levels previously assigned to the packets. The processing resources of the processor 114 are distributed in some form among all the queues vying for service. To distribute processing resource,

each queue is assigned a percentage of the processing capacity of the processor 114. For example, assuming 100% available resources, the time delay sensitive queues may be assigned a combined 80% of the resource while the non-delay sensitive queues are assigned the remaining 20%. The 80% can then be further broken down by priority level: class #4 corresponding to priority level P4, is assigned 5% of processing resources; class #3, corresponding to priority level P3, is assigned 10%; class #2, corresponding to priority level P2, is assigned 15%; and class #1, corresponding to priority level P1, is assigned 50%....the non-delay sensitive queue is assigned 20% of the processing resources);

Determining a plurality of precedence levels (class #1 through class #4) for at least a portion of information (packets) passing over communication network (see col. 12, lines 42-55, the order of retrieving packets from the queues 106, 108 is related to the various priority levels previously assigned to the packets. The processing resources of the processor 114 are distributed in some form among all the queues vying for service. To distribute processing resource, each queue is assigned a percentage of the processing capacity of the processor 114. For example, assuming 100% available resources, the time delay sensitive queues may be assigned a combined 80% of the resource while the non-delay sensitive queues are assigned the remaining 20%. The 80% can then be further broken down by priority level: class #4 corresponding to priority level P4, is assigned 5% of processing resources; class #3, corresponding to priority level P3, is assigned 10%; class #2, corresponding to priority level P2, is assigned 15%; and class

#1, corresponding to priority level P1, is assigned 50%....the non-delay sensitive queue is assigned 20% of the processing resources);

Assigning a percentage of buffer to each of precedence levels (class #1 through class #4), wherein the sum of percentage may exceed 100% (see col. 12, lines 42-55, the order of retrieving packets from the queues 106, 108 is related to the various priority levels previously assigned to the packets. The processing resources of the processor 114 are distributed in some form among all the queues vying for service. To distribute processing resource, each queue is assigned a percentage of the processing capacity of the processor 114. For example, assuming 100% available resources, the time delay sensitive queues may be assigned a combined 80% of the resource while the non-delay sensitive queues are assigned the remaining 20%. The 80% can then be further broken down by priority level: class #4 corresponding to priority level P4, is assigned 5% of processing resources; class #3, corresponding to priority level P3, is assigned 10%; class #2, corresponding to priority level P2, is assigned 15%; and class #1, corresponding to priority level P1, is assigned 50%....the non-delay sensitive queue is assigned 20% of the processing resources);

Receiving an information packets, packet having a label (class 178, 198, see figures 9, 10) indicating the precedence (class#1 through class#4) for transmitting information (see figure 6) (see col. 12, lines 34-36, the device 100 may comprise a plurality of time delay sensitive queues whereby each class (precedence levels) has associated with it one or more queues. In the example illustrated in FIG.6, class #1 through class #4 each have a single queue associated with them) (see col. 12, lines 42-55, the order of

retrieving packets from the queues 106, 108 is related to the various priority levels previously assigned to the packets. The processing resources of the processor 114 are distributed in some form among all the queues vying for service. To distribute processing resource, each queue is assigned a percentage of the processing capacity of the processor 114. For example, assuming 100% available resources, the time delay sensitive queues may be assigned a combined 80% of the resource while the non-delay sensitive queues are assigned the remaining 20%. The 80% can then be further broken down by priority level: class #4 corresponding to priority level P4, is assigned 5% of processing resources; class #3, corresponding to priority level P3, is assigned 10%; class #2, corresponding to priority level P2, is assigned 15%; and class #1, corresponding to priority level P1, is assigned 50%....the non-delay sensitive queue is assigned 20% of the processing resources);

Examining the label (class 178, 198, see figures 9, 10) on packet to determine the precedence level (class #1 through class #4) of packet; evaluating label (class 178, 198, see figures 9, 10) against plurality of precedence levels (class #1 through class #4); and If the precedence (class 178, 198) of packet matches one of plurality of precedence levels (class #1 through class #4), passing packet for processing in a priority buffer queue (see col. 12, lines 34-36, the device 100 may comprise a plurality of time delay sensitive queues whereby each class (precedence levels) has associated with it one or more queues. In the example illustrated in FIG.6, class #1 through class #4 each have a single queue associated with them) (see col. 12, lines 42-55, the order of retrieving packets from the queues 106, 108 is related to the various priority levels previously

assigned to the packets. The processing resources of the processor 114 are distributed in some form among all the queues vying for service. To distribute processing resource, each queue is assigned a percentage of the processing capacity of the processor 114. For example, assuming 100% available resources, the time delay sensitive queues may be assigned a combined 80% of the resource while the non-delay sensitive queues are assigned the remaining 20%. The 80% can then be further broken down by priority level: class #4 corresponding to priority level P4, is assigned 5% of processing resources; class #3, corresponding to priority level P3, is assigned 10%; class #2, corresponding to priority level P2, is assigned 15%; and class #1, corresponding to priority level P1, is assigned 50%....the non-delay sensitive queue is assigned 20% of the processing resources);

If the precedence of packet does not match one of plurality of precedence level (class #1 through class #4), passing packet for processing in at least one other output queue (non-delay sensitive queue, see figure 6) (see col. 12, lines 34-36, the device 100 may comprise a plurality of time delay sensitive queues whereby each class (precedence levels) has associated with it one or more queues. In the example illustrated in FIG.6, class #1 through class #4 each have a single queue associated with them) (see col. 12, lines 42-55, the order of retrieving packets from the queues 106, 108 is related to the various priority levels previously assigned to the packets. The processing resources of the processor 114 are distributed in some form among all the queues vying for service. To distribute processing resource, each queue is assigned a percentage of the processing capacity of the processor 114. For example, assuming 100% available

resources, the time delay sensitive queues may be assigned a combined 80% of the resource while the non-delay sensitive queues are assigned the remaining 20%. The 80% can then be further broken down by priority level: class #4 corresponding to priority level P4, is assigned 5% of processing resources; class #3, corresponding to priority level P3, is assigned 10%; class #2, corresponding to priority level P2, is assigned 15%; and class #1, corresponding to priority level P1, is assigned 50%....the non-delay sensitive queue is assigned 20% of the processing resources);

However, Rochberger et al. is silent to disclosing transmitting any information in priority queue before transmitting any information in at least one other output buffer queue.

See figure 28, Dravida et al. (U.S.Patent No. 2002/0105965 A1 "Provisional application No. 60/234,682, filed on Sep. 22, 2000") discloses there are four QoS classes (precedence levels) in the embodiment of the Access Network, there are four egress buffers—one for each class—in each NIU. Each egress buffer is allocated a fixed amount of space to hold packets. The egress buffer control stage 1310 performs a simple operation. When a packet is handed to this stage, it checks if the egress buffer associated with the packet's QoS class (which is a function of its service instance) has adequate space (in term of byte count) to hold the packet, see page 18, [0258]); comprising:

transmitting any information in priority queue before transmitting any information in at least one other output buffer queue (see page 19, [0277], after finishing copying a packet into a transmit buffer, the scheduler scans the input queues going from the

highest priority to the lowest priority queue to see which is the highest priority packet waiting at the head of its queue which is ready for transmission);
determining a maximum packet size; if the received information packet exceeds the maximum packet size, discarding the packet (see page 18, [0025], packet size restriction can also be enforced at this stage. For instance, if a service instance is set up with a limit on the maximum packet size, a packet belonging to that service instance can be dropped at this stage if it size exceeds the corresponding limit...packet size restrictions may be enforced at the traffic policing stage).

Thus, it would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Rocchberger with the teaching of Dravida to transmitting any information in priority queue before transmitting any information in at least one other output buffer queue in order to speed up forwarding.

9. In the claim 5, Rochberger discloses communication network is a packet based network (see figures 9, 10).

10. In the claim 6, Dravida discloses determining a maximum packet size; if the received information packet exceeds the maximum packet size, discarding the packet (see page 18, [0025], packet size restriction can also be enforced at this stage. For instance, if a service instance is set up with a limit on the maximum packet size, a packet belonging to that service instance can be dropped at this stage if it size exceeds the corresponding limit...packet size restrictions may be enforced at the traffic policing stage).

11. In the claim 7, Rochberger et al. discloses information is transmitted in data packet and each data packet includes a packet header (see figures 9, 10).

12. In the claim 8, Rochberger et al. discloses the data having an indication for the precedence (class 178, 198, figures 9, 10) for transmitting information is included in a field in packet header (see figures 9, 10).

13. Claims 15, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined system (Rochberger – Dravida) in view of Ganti et al. (U.S.Patent No. 2003/0185217 "Filed March 28, 2002).

In the claims 15, 9, Rochberger discloses the limitations "field comprises a type of service (class of service 178, 198, figures 9, 10).

However, the combined system (Robechberger – Dravida) is silent to disclosing label comprises a differentiated services code point within type of service field.

Ganti discloses a differentiated services code point within type of service field (see page 5, [0075], the per-class advertisements correspond to the Diffserv PHE Scheduling Classes).

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined system (Robechberger – Dravida) with the teaching of Ganti to provide a differentiated services code point within type of service field in order to set up a connection for several classes of traffic.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong ho whose telephone number is (571)272-3133. The examiner can normally be reached on Monday-Friday from 8:00AM-4:00PM.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

12/08/04